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UTILITY APPLICATION FOR UNITED STATES PATENT  
FOR  
METHOD FOR FABRICATING CAPACITOR IN SEMICONDUCTOR DEVICE

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# METHOD FOR FABRICATING CAPACITOR IN SEMICONDUCTOR DEVICE

## Field of Invention

5           The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to a method for fabricating a capacitor in a semiconductor memory device.

## 10   Description of Related Art

          Due to large-scale integration of semiconductor devices, for instance, a dynamic random access memory (DRAM), the total area of a memory cell for storing  
15   information, has rapidly decreased.

          Particularly, the reduced memory cell area reduces the available area for a capacitor in the memory cell. The reduced memory cell area also reduces a sensing margin and a sensing speed. Furthermore, this reduction of the  
20   memory cell area lessens tolerance to soft errors, of the type created by  $\alpha$  particles.

          A capacitance C of a capacitor is defined by the following equation.

$$25 \qquad C = \epsilon \times A_s/d \qquad \text{Eq. 1}$$

          Herein,  $\epsilon$  is a dielectric constant;  $A_s$  is an effective surface area of a electrode; d is a distance between the electrodes.

30           Based on the Eq. 1, there are three approaches for increasing the capacitance of the capacitor: the first approach is to increase the effective surface area of the electrode; the second approach is to decrease a thickness

of a dielectric substance; and the third approach is to increase the dielectric constant.

Among the three approaches, the first approach is initially considered for increasing the capacitance of the capacitor. As mentioned above, in the first approach, the effective surface area of the electrode is increased. Thus, the capacitor should be formed with a specific three-dimensional structure such as a concave structure, a cylinder structure, a multiply layered pin structure and so on. However, this approach has become limited due to a trend of ultra large-scale integration of a semiconductor device.

The second approach is to decrease the thickness of the dielectric substance to minimize a distance  $d$  between the electrodes. This approach is also faced with a limitation because leakage currents are increased due to the fact that the thickness of the dielectric substance is decreased.

Therefore, current research and development focuses on how to increase the capacitor capacitance by increasing the dielectric constant. Most capacitors have a so-called nitride-oxide(NO) structure wherein a silicon oxide layer and a silicon nitride layer are used for the dielectric layer. However, the dielectric layer for the capacitor is made of a material having a high dielectric constant as  $\text{Ta}_2\text{O}_5$ ,  $(\text{Ba},\text{Sr})\text{TiO}_3$  (BST) and the like or a ferroelectric material as  $(\text{Pb},\text{Zr})\text{TiO}_3$  (PZT),  $(\text{Pb},\text{La})(\text{Zr},\text{Ti})\text{O}_3$  (PLZT),  $\text{SrBi}_2\text{Ta}_2\text{I}_9$  (SBT),  $\text{Bi}_4\text{-XLaXTi}_3\text{O}_{12}$  (BLT) and the like.

Figs. 1A to Fig. 1C are cross-sectional views showing a conventional method for fabricating a capacitor with a cylinder structure.

As shown in Fig. 1A, an active region 11 is formed in a substrate 10. After an inter-insulation layer 12 is

formed on substrate 10, a contact hole is formed for contacting the active region 11 of the substrate 10 by passing through the inter-insulation layer 12. The contact hole is buried with a conductive metal to form a contract plug 13. Then, an insulation layer 14 is formed with the same height as that of the capacitor.

The insulation layer 14 is selectively etched to expose the contact plug 13 to form a trench. A bottom electrode 15 is formed with a conductive silicon layer and is deposited along a profile containing the trench. Then, the insulation layer 14 is eliminated.

As shown in Fig. 1B, a silicon nitride layer 16 is formed with a thickness ranging from about 5 Å to about 50 Å on the bottom electrode 15 by using ammonia (NH<sub>3</sub>) plasma. Referring to Fig. 1C, a dielectric layer 17 is formed on the silicon nitride layer 16, and a top electrode is formed thereon by employing the conductive layer.

Herein, the silicon nitride layer 16 is formed for preventing formation of a silicon oxide layer during a subsequent high thermal process. If the silicon oxide layer having a low dielectric constant is formed above and below the dielectric layer, the dielectric characteristic of the capacitor is deteriorated.

The silicon nitride layer 16 is not uniformly formed on a surface of the bottom electrode 15 because the bottom electrode 15 has a cylinder structure. Hence, the silicon oxide layer is excessively formed on a portion of the bottom electrode 15 on which the silicon nitride layer 16 is not formed. As a result, there arises a problem that the capacitance is decreased on some portions of the bottom electrode 15 due to the excessive formation of the unintended silicon oxide formation.

In addition, the nitride layer for preventing a

reduction of the capacitance creates a problem because a current leakage in the capacitor is increased and a breakdown voltage is decreased.

## 5 Summary of Invention

It is, therefore, an object of the present invention to provide a method of fabricating a capacitor of a semiconductor device to improve a capacitance and  
10 concurrently enhance a leakage current characteristic and a breakdown voltage characteristic.

In accordance with an aspect of the present invention, there is provided the method for fabricating the capacitor of a semiconductor device, including the  
15 steps of: (a) forming a conductive silicon layer for a bottom electrode on a substrate; (b) nitridating the conductive silicon layer; (c) oxidizing the nitridated conductive silicon layer; (d) forming a silicon nitride layer on a surface of the oxidized layer; (e) forming a  
20 dielectric layer on the silicon nitride layer; and (f) forming a top electrode on the dielectric layer.

## Brief Description of the Drawings

25 The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1A to Fig. 1C are cross-sectional views showing  
30 a conventional method for fabricating a capacitor with a cylinder structure;

Figs. 2A to Fig. 2E are cross-sectional views showing a method for fabricating a capacitor of a semiconductor

device in accordance with a preferred embodiment of the present invention; and

Figs. 3A to Fig. 3C are graphs showing effectively established characteristics of the capacitor fabricated in accordance with the present invention.

#### Detailed Description of the Invention

Hereinafter, a capacitor of a semiconductor device fabricated in accordance with the present invention will be described in detail referring to the accompanying drawings.

Figs. 2A to 2E are cross-sectional views showing a method for fabricating a capacitor of a semiconductor device in accordance with a preferred embodiment of the present invention.

As shown in Fig. 2A, an active region 21 is formed in a substrate 20. After an inter-insulation layer 22 is formed on a substrate 20, a contact hole is formed by passing through the inter-insulation layer 22 so that a plug 23 contacts the active region 21 of the substrate 20. The contact hole is filled with a conductive metal to form the plug 23. Hereinafter, this plug 23 is referred to as a contact plug. The inter-insulation layer 22 is formed with an oxide layer or a thermal oxide layer. The oxide layer is made of a material selected from a group consisting of undoped-silicate glass (USG), phosphorus-silicate glass (PSG), boron-phosphorus-silicate glass (BPSG), high density plasma (HDP), spin on glass (SOG) and tetra-ethyl-ortho silicate (TEOS). The thermal oxide layer is formed by oxidizing a silicon substrate at a temperature ranging from about 600°C to about 1100°C.

An insulation layer 24 is formed in the same height

of the capacitor. The insulation layer 24 is formed with a thickness ranging from about 3000 Å to about 5000 Å by employing an oxide layer or a thermal oxide layer.

Herein, the oxide layer and the thermal oxide layer are  
5 formed with the same method as described above.

Next, the insulation layer 24 is selectively etched until the contact plug 23 is exposed so that a trench is formed. A bottom electrode 25 is formed along a profile containing the trench. At this time, the bottom electrode  
10 25 is made of polysilicon.

Describing in further detail the bottom electrode 25 formation, an impurity doped polysilicon layer is deposited with a thickness ranging from about 50 Å to about 300 Å. An impurity non-doped polysilicon layer is  
15 subsequently deposited to a thickness ranging from about 50 Å to about 300 Å, and phosphine ( $\text{PH}_3$ ) is then doped thereon in an atmosphere of nitrogen ( $\text{N}_2$ ).

Referring to Fig. 2B, the insulation layer 24 for a capacitor is removed and a SC-1 cleaning process is  
20 performed thereafter. At this time, the hydrofluoric acid (HF) or buffer oxide etchant (BOE) is used in the SC-1 cleaning process to remove the insulation layer 24. The SC-1 cleaning process also employs ammonium hydroxide ( $\text{NH}_4\text{OH}$ ), hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) and  $\text{H}_2\text{O}$ . As a result of  
25 the SC-1 cleaning process, a first silicon oxide layer 26 of which thickness ranges from about 5 Å to about 10 Å is formed in a manner to encompass the bottom electrode 25. When the SC-1 cleaning process is performed, the first silicon oxide layer 26, which is a thin native oxide layer  
30 formed during the SC-1 cleaning process, is formed in a thickness ranging about 5 Å to about 10 Å.

Afterwards, the polysilicon layer formed as the bottom electrode 25 is doped with  $\text{PH}_3$  in an atmosphere of

N<sub>2</sub>. At this time, the doping is performed at a temperature ranging from about 500 °C to about 800 °C and a pressure ranging from about 0.1 Torr to about 100 Torr. This doping is to minimize a depletion phenomenon occurring  
5 during operation of the capacitor.

Then, a thermal treatment process is performed. This process densifies the first silicon oxide layer 26 to a greater extent and minimizes oxidization of the bottom electrode 25 during the thermal treatment process  
10 performed with use of a furnace in an atmosphere of N<sub>2</sub>O after a dielectric layer deposition process.

As shown in Fig. 2C, a first silicon nitride layer 27 is uniformly formed by the thermal treatment process which is carried out in a pressure ranging from about 10 Torr to  
15 about 100 Torr with use of a furnace.

Referring to Fig. 2D, a second silicon oxide layer 28 is formed on the first silicon nitride layer 27 by exposing the substrate 20 to an atmosphere. At this time, a thickness of the second silicon oxide layer 28 ranges  
20 from about 1 Å to about 5 Å. The second silicon oxide layer 28 is a native oxide layer generated when the substrate 20 is exposed in the atmosphere.

A second silicon nitride layer Si<sub>3</sub>N<sub>4</sub> 29 is deposited by using a dichlorosilane (DCS) source in an atmosphere of  
25 NH<sub>3</sub> and at a pressure ranging from about 1 Torr to about 10 Torr. Herein, the first and the second silicon nitride layers 27 and 29 are formed in a thickness ranging from about 5 Å to about 20 Å.

As shown in Fig. 2E, on the second silicon nitride layer 29, a dielectric layer 30 is formed in a thickness  
30 ranging from about 30 Å to about 100 Å. At this time, a temperature for forming the dielectric layer 30 ranges from about 300 °C to about 500 °C. Also, the dielectric



layer 30 is formed under a pressure ranging from about 0.1 Torr to about 1.0 Torr. For improving device characteristics and crystallization of the dielectric layer 30, a thermal treatment process is performed in an atmosphere of  $N_2O$  or  $O_2$  with use of a furnace. At this time, the thermal treatment process is carried out at a temperature ranging from about 500 °C to about 800 °C.

In case of using  $Ta_2O_5$  for forming the dielectric layer 30, the dielectric layer is formed by using  $Ta(C_2H_5O)_5$  and  $O_2$  as a source and a reaction gas. At this time, the dielectric layer 30 formation is carried out at a temperature ranging from about 300 °C to about 500 °C and a pressure ranging from about 0.1 Torr to about 1.0 Torr. Also, a thickness of the dielectric layer 30 ranges from about 20 Å to about 100 Å. The dielectric layer 30 is made of a material selected from a group of substances having a high dielectric constant such as  $Al_2O_3$ ,  $HfO_2$ , BST and so on or a group of ferroelectric substances such as PZT, PLZT, BLT and so on.

Next, a top electrode 31 is formed on the dielectric layer 30 by using a conductive layer. The top electrode 31 is formed by depositing a TiN layer through the use of chemical vapor deposition (CVD) and then a polysilicon layer on the top electrode 31.

The first silicon nitride layer 27, the second silicon oxide layer 28 and the second silicon nitride layer 29 are formed between the dielectric layer 30 and the bottom electrode 29 by employing the process as described above. This process is called a second effective furnace nitridation (EF2N) process. Herein, the first and second silicon nitride layers 27 and 29 is to prevent the oxide layer from being excessively generated in order to secure a predetermined capacitance, and the

second silicon oxide layer 28 is for improving a leakage current characteristic and a breakdown voltage characteristic.

5 Figs. 3A to 3C are graphs showing effectively established characteristics of the capacitor fabricated in accordance with the present invention.

Especially, the graphs present characteristics about capacitance  $C_s$ , leakage current and breakdown voltage of the capacitors obtained under a conventional  $\text{NH}_3$  plasma process for suppressing the formation of the oxide layer on an interface between dielectric layers and the  
10 aforementioned EF2N process for suppressing the formation of the oxide layer on interface between the bottom electrode and the dielectric layer.

15 Referring to Figs. 3A and 3B, compared with the capacitance of a capacitor fabricated by the conventional  $\text{NH}_3$  plasma process ( $\text{NH}_3$  PLT), the capacitance  $C_s$  is improved by using the EF2N process. In addition, characteristics of leakage current and breakdown voltage  
20 are constantly maintained.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modification may be made without departing from the spirit  
25 and scope of the invention as defined in the following claims.